DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Scheme of Instruction, Evaluation

and

Syllabi of

B.E. HONOR

in

VLSI DESIGN

With effect from Academic Year 2024-25

UNIVERSITY COLLEGE OF ENGINEERING
(Autonomous)

Osmania University

Hyderabad – 500 007, TS, INDIA

With effect from Academic Year 2024-25

SCHEME OF INSTRUCTION AND EXAMINATION

Scheme and Syllabus for

B.E. HONORS IN VLSI DESIGN

SNo	Code	Course Title	Scheme of Instruction			Contact Hrs/Wk	Scheme of Evaluation			Credits
			L	T	P		Hrs	CIE	SEE	
Theory										
1	HR501EC	Advanced System Design	3	-	-	**3**	3	40	60	3
2	HR601EC	Fundamentals of System Verilog	3	-	-	**3**	3	40	60	3
3	HR602EC	Design for Testability	3	-	-	3	3	40	60	3
4	HR701EC	Intelligent CAD	3	-	-	**3**	3	40	60	3
5	HR702EC	CMOS Analog and Mixed Signal IC Design	3	-	-	**3**	3	40	60	3
6	HR851EC	HR-Project Work	-	-	6	**6**	-	-	100	3
		Total	**15**	**-**	**6**	**21**	**15**	**200**	**400**	**18**

Course Code	Course Title						Core/PE/OE
HR501EC	**Advanced System Design**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
-	L	T	D	P			
	3	-	-	-	40	60	**3**

Course Objectives

1. The objectives of this course are to provide knowledge on
2. To understand the concept of various casting processes & furnaces.
3. To gain knowledge on various metal forming processes like rolling & extrusion.
4. To know the principle of forging and various press working operations.
5. To familiarize the different techniques of joining processes.
6. To understand the manufacturing of plastics, powder metallurgy and composites.

Course Objectives

After completing this course, the student will be able to:

1. Understand the basic working principles of casting, forming and welding.
2. Some understanding of types, manufacturing processes and applications of plastics and composite materials.
3. Recommend appropriate part manufacturing processes when provided a set of functional requirements.
4. Ability to analyze problems on forging, rolling, drawing and extrusion.
5. Communicate effectively with industry personnel by developing a manufacturing-centric vocabulary.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	2	1	2	-	-	-	-	-	-	1
CO2	2	2	2	1	2	-	-	-	-	-	-	1
CO3	3	2	3	2	3	-	-	-	1	-	-	1
CO4	3	2	3	2	3	-	-	-	1	1	-	1
CO5	1	2	3	1	2	-	-	-	2	1	-	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I:

Introduction to Advanced System Design (ARM Cortex IP): The ARM RISC design philosophy, System hardware – AMBA bus, System software; ARM registers bank, status registers; vector table, data flow model.

UNIT-II:

Cortex M4 SoC Architecture: Cortex M SoC Processor: introduction – Block diagram; Interrupts and Processor Reset Sequence.CortexM4, STM32F features; Memory Map; ARM Bus Matrix; Nested Vectored Interrupt Controller (NVIC), Interrupts Vs Exceptions; Cortex M Processor Modes.

UNIT-III:

ARM Instruction Set Architecture (ARM ISA): Fundamentals of ARM instructions, ARM Assembly instructions: Data processing, Branching, Load-store, SWI and Program Status Register instruction. Thumb ISA.

UNIT-IV:

SoC Programming (STM32F): GPIO Management: Accessibility & Configurations; Timer Programming; UART: Configuration, baud rate generation, UARTx drivers in C; I2C: Features, modes, Pins and Registers; I2C Driver Programming; SPI: master/slave operation, Pins & Registers; ADC Driver for data sampling & processing needs.

UNIT-V:

ARM Interfacing with Real World: Interfacing of switches, LEDs; Seven Segment Display; Matrix Keypad; LCD – Design options; DC Motor & Stepper Motor interfacing designs in Embedded C/C++; debugging methods.

Suggested Reading

1. ARM System-on-chip Architecture by Steve Furber, Pearson Education, ISBN978-81-317-0840-8, 2E, 2012.
2. STM32 ARM Programming for Embedded Systems, Muhammad Ali Mazidi, Shujen Chen, Eshragh Ghaemi ISBN: 978-099-792-5944, 2018
3. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®-M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC.

Course Code	Course Title						Core/PE/OE
HR601EC	**Fundamentals of System Verilog**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	**3**

Course Objectives: The course is taught with the objectives of enabling the student to:

1. To Know Basics of System Verilog
2. To Familiarize with Object Oriented Programming
3. To Explore Randomization and Threads in System Verilog
4. To Know Test Coverage in System Verilog

Course Objectives : On completion of the course, students will be able to

1. To understand the basic concepts of Design Verification
2. To Construct User Defined Data Types in System Verilog
3. To Create Object Oriented Programming Environment
4. To Create Object Oriented Programming Environment
5. To understand the Coverage Concepts

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	2	-	-	-	-	-	-	-	-	-
CO2	1	1	2	2	3	-	-	-	-	-	-	1
CO3	1	2	2	2	3	-	-	-	-	-	-	1
CO4	1	2	2	2	3	-	-	-	-	-	-	1
CO5	1	2	2	2	3	-	-	-	-	-	-	1

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I:

Verification Guidelines: Introduction, Verilog vs System Verilog, Verification Process , Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Testbench Components, Layered Testbench, Building a Layered Testbench, Simulation Environment Phases

UNIT-II:

DATA TYPES: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, choosing a Storage Type, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings, Net Types

Tasks & Functions: Tasks, Functions, and Void Functions, Routine Arguments, Local Data Storage, Time Values, Procedural Statements

UNIT-III:

Basic OOP concepts: Object Oriented Programming significance and advantages, classes, objects, objecthandles, methods, Static and Global Variables, using one class inside another class, Dynamic objects, copying objects, Public Vs Local and Building a test bench. Inheritance, Overriding, Data Hiding and Encapsulation, Abstract Classes and Virtual Methods. Scope Resolution Operator, Classes Extern Methods, type def classes

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UNIT-IV:

Randomization: Randomization in System Verilog, Constraint Details,, Solution Probabilities, Controlling Multiple Constraint Blocks, Valid Constraints, In-line Constraints, The pre_randomize and post randomize Functions, Common Randomization Problems, Iterative and Array Constraints

THREADS AND INTERPROCESS COMMUNICATION: Interprocess Communication, Events, Semaphores, Mailboxes.

UNIT-V:

Coverage: Introduction to Coverage, Coverage Types, Functional Coverage Strategies, Anatomy of a Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage

Introduction to Universal Verification Methodology (UVM)

Suggested Reading

1 Christ Spear and Greg Tumbush, System Verilog for Verification, 3 rd ed., Springer, 2012

2 Gamma, Erich, Helm, Richard, Johnson, Ralph, and Vissides, John, Design Patterns: Elements of Reusable Object-Oriented Software. Reading, MA: Addison-Wesley 1995

3 Sutherland, Stuart, Davidmann, Simon, and Flake, Peter. SystemVerilog for Design. Norwell, MA: Kluwer Academic Publishers, 2004

Course Code	Course Title						Core/PE/OE
HR602EC	**Design for Testability**						**Core**
Prerequisite	**Contact Hours Per Week**				CIE	SEE	Credits
DSD	L	T	D	P			
	3	-	-	-	40	60	**3**

Course Objectives: The course is taught with the objectives of enabling the student to:

1. To Understand testability fundamentals and fault models
2. To understand the significance of fault simulation
3. To understand test generation for SSFs
4. To learn about scan architectures
5. To understand specific and random BIST.

Course Objectives: On completion of this course, the student will be able to :

1. Understand modeling at various abstraction levels , delay and logic simulation
2. Understand fault classes and their models
3. Understand and apply test generation algorithms for SSFs
4. Understand boundary scan standards
5. Understand BIST architectures

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	2	-	-	-	-	-	-	-	-	-	-	1	-	-
CO2	2	-	-	-	-	-	-	-	1	-	-	1	2	-
CO3	2	2	2	-	-	-	-	-	1	-	-	1	2	-
CO4	2	2	-	-	-	-	-	-	1	-	-	1	2	-
CO5	2	1	-	-	-	-	-	-	-	-	-	1	1	-

Correlation rating: Low / Medium / High: 1 / 2 / 3 respectively

UNIT-I

Introduction to Test and Design for Testability (DFT): Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural level.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation

UNIT-II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits

Unit -III

Test Generation algorithms for SSFs: Combinational Circuits-Fault oriented ATG- algorithms and selection criteria, fault independent ATG, ATG for sequential circuits using iterative array model.

UNIT-IV

Design for testability: Testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards.

UNIT-V

Built In Self-Test (BIST): BIST concepts, Specific BIST architectures – CSBL, BILBO, Random logic BIST-BIST process- Pattern generation – Response compaction , Circuit initialization, Test point insertion.

Suggested Reading

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002
3. Robert J. Feugate, Jr., Steven M. Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998
4. Parag. K. Lala, "Fault tolerant and fault testable hardware design",BS Publications, 2002